PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Group Art Unit: 2827

Application No.: 09/486,561

Examiner: L. Cruz

Filed: February 29, 2000

Docket No.: 105030

For: SEMICONDUCTOR DEVICE AND METHOD THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the August 14, 2002 Office Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 4 and 10 without prejudice to or disclaimer of the subject matter contained therein.

Please replace claims 1, 8, 11, 12 and 14-16 as follows:

1. (Three Times Amended) A method of manufacturing a semiconductor device comprising:

a first step of interposing an adhesive between a surface of a substrate on which an interconnect pattern is formed and a surface of a semiconductor chip on which electrodes are formed, said adhesive having conductive particles dispersed therein; and

a second step in which pressure is applied between said semiconductor chip and said substrate, said interconnect pattern and said electrodes are electrically connected via said conductive particles of said adhesive, and said adhesive is caused to cover substantially all of a lateral surface of said semiconductor chip.

8. (Three Times Amended) A semiconductor device, comprising:

a semiconductor chip having electrodes; a substrate having an interconnect pattern; and an adhesive, said adhesive having conductive particles dispersed therein;

wherein said electrodes and said interconnect pattern are electrically connected via said conductive particles of said adhesive; and

wherein said adhesive is interposed between a surface of said substrate on which said interconnect pattern is formed and a surface of said semiconductor chip on which said electrodes are formed, and said adhesive covers substantially all of a lateral surface of said semiconductor chip.

11. (Twice Amended) The semiconductor device as defined in claim 8, wherein said adhesive is provided to cover said interconnect pattern in its entirety.

12. (Amended) The semiconductor device as defined in claim 8,

wherein said adhesive includes a shading material.

14. (Twice Amended) A circuit board on which is mounted a semiconductor device, the semiconductor device comprising:

a semiconductor chip having electrodes; a substrate having an interconnect pattern; and an adhesive, said adhesive having conductive particles dispersed therein;

wherein said electrodes and said interconnect pattern are electrically connected via said conductive particles of said adhesive; and

wherein said adhesive is interposed between a surface of said substrate on which said interconnect pattern is formed and a surface of said semiconductor chip on which

said electrodes are formed, and said adhesive covers substantially all of a lateral surface of said semiconductor chip.

15. (Twice Amended) An electronic instrument having a semiconductor device, the semiconductor device comprising:

a semiconductor chip having electrodes; a substrate having an interconnect pattern; and an adhesive, said adhesive having conductive particles dispersed therein;

wherein said electrodes and said interconnect pattern are electrically connected via said conductive particles of said adhesive; and

wherein said adhesive is interposed between a surface of said substrate on which said interconnect pattern is formed and a surface of said semiconductor chip on which said electrodes are formed, and said adhesive covers substantially all of a lateral surface of said semiconductor chip.

16. (Amended) The semiconductor device as defined in claim 8, wherein at least a part of said adhesive has a thickness substantially the same as said semiconductor chip.

REMARKS

Claims 1, 2, 5-8, 11, 12, 14-16, 21 and 22 are pending herein, with non-elected claims 1, 2 and 5-7 being withdrawn from consideration by way of a Restriction Requirement.

By this Amendment, claims 1, 8, 11, 12 and 14-16 are amended and claims 4 and 10 are canceled.

More in particular, each of independent claims 1, 8, 14 and 15 is amended to recite that the adhesive includes conductive particles dispersed therein, which conductive particles participate in the electrical connection between the electrodes and the interconnect pattern. The amended claims distinguish the claimed invention from the teachings of Yamada as discussed more fully below. Support for these amendments to the claims may be found throughout the original specification, including original claims 4 and 10.

Claim 11 is amended to revise its dependency in view of the cancellation of claim 10, and also for consistency in referring back to claim 8. Claim 12 is amended to revise its dependency. Finally, claim 16 is amended for consistency with the language of claim 8 in order to overcome the rejection under 35 U.S.C. §112, second paragraph.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration, because the amendments to the independent claims merely incorporate therein limitations previously considered by the Patent Office in dependent claims 4 and 10; (c) satisfy a requirement of form asserted in the previous Office Action; (d) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (e) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

In view of the foregoing amendments and the following remarks, reconsideration of this application is respectfully requested.

Applicant appreciates the courtesies shown to Applicant's representative by Examiner Cruz in the December 4, 2002 interview. Applicant's separate record of the substance of the interview is incorporated into the following remarks.

I. Rejection Under 35 U.S.C. §112, Second Paragraph

Claim 16 was rejected under 35 U.S.C. §112, second paragraph as allegedly being indefinite. This rejection is respectfully traversed.

By this Amendment, claim 16 has been amended so that the term "said second portion" is replaced with a term having proper antecedent basis in claim 8 from which claim 16 depends. Thus, claim 16 should now fully comply with the requirements of 35 U.S.C. §112, second paragraph.

For the foregoing reasons, reconsideration and withdrawal of this rejection are respectfully requested.

II. Rejection Under 35 U.S.C. §102(e)

Claims 8, 10, 11, 14-16, 21 and 22 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 5,864,178 (hereinafter Yamada). This rejection is respectfully traversed.

Yamada describes a semiconductor device comprising a wiring circuit board and a semiconductor chip mounted through a bump electrode on the circuit board, a space between the circuit board and the semiconductor chip as well as a periphery of the semiconductor chip being encapsulated with a resin containing a filler. The resin is constituted by a first resin disposed in a region surrounded by bump electrodes positioned on the outermost periphery of the semiconductor chip, and by a second resin disposed in a region not surrounded by bump electrodes positioned on the outermost periphery of the semiconductor chip, the first and second resins being distinct from each other in at least one feature selected from a content, a maximum particle diameter and an average particle diameter of the filler. See the Abstract.

Yamada thus describes that the semiconductor chip is bonded to the wiring circuit board via bump electrodes. The strength of the device is then enhanced by encapsulating the chip and connection with a thermosetting resin. The thermosetting resin includes a non-conductive, inorganic filler (silica or quartz) (see column 21, line 63 to column 22, line 5 of Yamada) therein in order to adjust properties of the resin associated with strength (e.g., coefficient of thermal expansion, elastic modulus, etc.) of the resin. See column 14, lines 1-

68 of Yamada. That is, the filler is included to adjust the resin to have properties increasing the resistance of the device to stress.

Yamada thus uses the resin as a protecting encapsulant, not as an adhesive to bond the semiconductor chip to the wiring circuit board.

Yamada thus fails to teach or suggest a semiconductor chip having electrodes, a substrate having an interconnect pattern and an adhesive comprising a binder having conductive particles dispersed therein, wherein the electrodes and the interconnect pattern are electrically connected via the conductive particles of the adhesive, and wherein the adhesive is interposed between a surface of the substrate on which the interconnect pattern is formed and a surface of the semiconductor chip on which the electrodes are formed, the adhesive covering substantially all of a lateral surface of the semiconductor chip as required in each of independent claims 1, 8, 14 and 15 of the present application.

Yamada does not teach or suggest that the resin encapsulant include conductive particles. Instead, Yamada teaches that the inorganic filler should be quartz, silica and the like that can improve the strength characteristics of the resin encapsulant.

Further, Yamada does not teach or suggest that electrical connection between the interconnect pattern and the electrodes of the semiconductor chip is made via the conductive particles of the adhesive. Yamada teaches only that the electrical connection between the wiring circuit board and the semiconductor chip is effected through the bump electrode, and not through any aspect of the resin encapsulant. The resin encapsulant in Yamada is used solely for strength purposes, and does not participate in electrical connections within the device.

Finally, for completeness, Applicant stresses that not only does Yamada fail to anticipate the claimed invention for all of the reasons set forth above, Yamada also would not have led one of ordinary skill in the art to the presently claimed invention. Again, Yamada

does not teach or suggest the use of conductive particles at all, and moreover does not teach or suggest that the resin and inorganic filler must participate in the electrical connection of the interconnect pattern and electrodes of the semiconductor chip. Thus, nothing in Yamada would have motivated one of ordinary skill in the art to have included conductive particles in the resin encapsulant of Yamada.

Further, if such conductive particles were to be included in the resin encapsulant of Yamada, the presence of the conductive particles would actually interfere with the bump electrode electrical connection by potentially shorting such connection (the conductive particles in the encapsulant of Yamada forming a potentially undesired electrical path therein). Thus, a practitioner in the art would have been led away from including conductive particles in the resin encapsulant of Yamada.

For at least the foregoing reasons, Applicant submits that Yamada does not teach or suggest the presently claimed invention. Reconsideration and withdrawal of this rejection are respectfully requested.

III. Rejection Under 35 U.S.C. §103(a)

Claim 12 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Yamada in view of U.S. Patent No. 5,783,465 (Canning). This rejection is respectfully traversed.

The Patent Office referred to Canning as allegedly teaching including a shading pigment in the material of Yamada. Even if this were accepted, it is clear that Canning does not remedy the deficiencies of Yamada discussed extensively above.

Accordingly, Applicant respectfully submits that neither Yamada nor Canning, whether taken singly or in combination, teaches or suggests the claimed invention. Reconsideration and withdrawal of this rejection are requested.

IV. Rejoinder

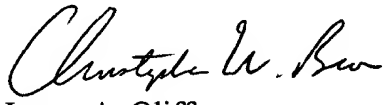
Applicant submits that upon allowance of claims 8, 11, 12, 14-16, 21 and 22, claims 1, 2 and 5-7, drawn to a method of making the semiconductor device of claim 8, must be rejoined and similarly allowed.

V. Conclusion

In view of the foregoing amendments and remarks, Applicant submits that claims 1, 2, 5-8, 11, 12, 14-16, 21 and 22 are in condition for allowance.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,



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Attachment:
Appendix

Date: December 6, 2002

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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
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